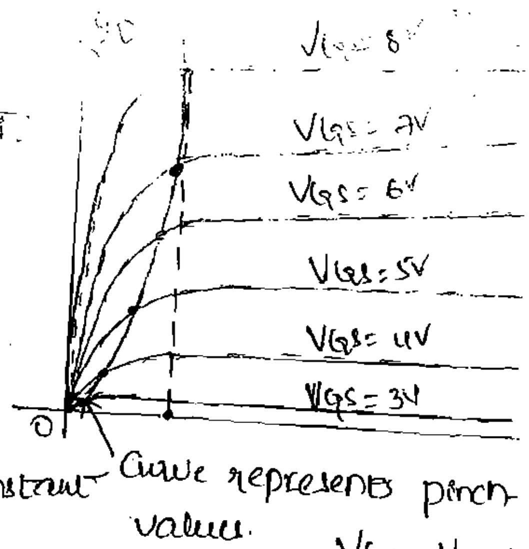
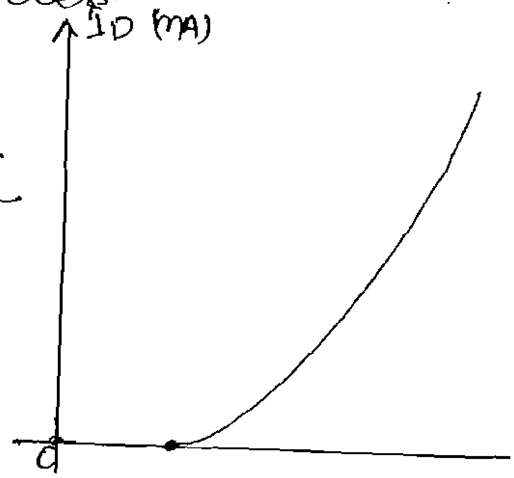
The fig shows the drain characteristics of an n-channel Enhancement type MOSFET. We can say that VGS increases beyond threshold value, the density of free carriers (electrons) in the induced channel increases, increasing the drain current. However at some point of VDS, for constant VGS, the drain current reaches a saturation level. The value of VDS at this point is known as pinch-off voltage (Vp). The levelling off of ID is due to a pinch-off process.



The characteristics of transfer is quite different from that obtained for JFET and depletion type MOSFET. We know that ID does not flow until $V_{GS}=V_T$

for $V_{GS}>V_T$ the relationship b/w drain current and VGS is non linear & given as $I_D = K(V_{GS}-V_T)^2$ & K-constant $= \dfrac{I_{D(ON)}}{(V_{GS(ON)}-V_T)^2}$

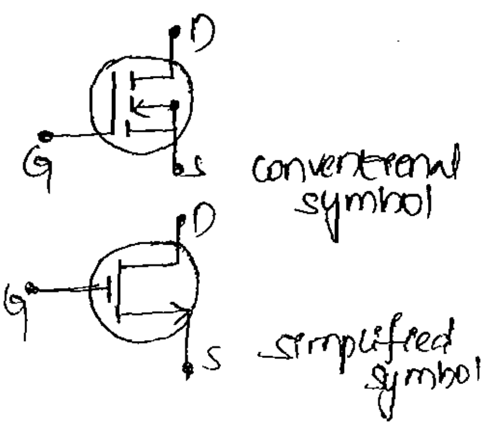


K → conduction parameter, given as $K = \dfrac{W\mu_n C_{ox}}{2L}$

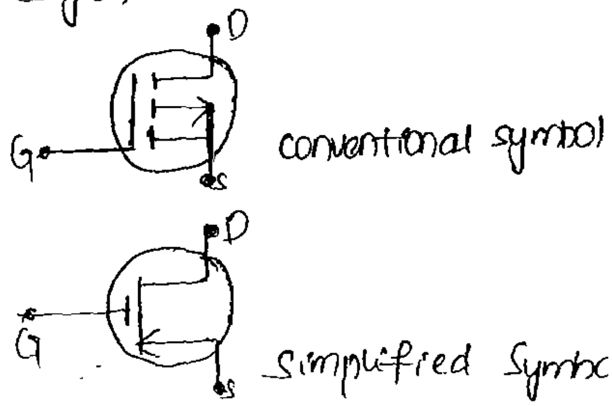
C_{ox} → oxide capacitance per unit area; $C_{ox} = \dfrac{\epsilon_{ox}}{t_{ox}}$

t_{ox} → oxide thickness; ϵ_{ox} is the oxide permittivity.

W → channel width, L → channel length.



n-channel Enhancement type MOSFET



p-channel Enhancement type MOSFET

Transistor Biasing and thermal stabilization

Region of operation	Emitter Base junction	collector Base junction
Cutoff	Reverse biased	Reverse biased.
Active	forward biased	Reverse biased
Saturation	forward biased	forward biased.

In order to operate transistor in the desired region we have to apply External d.c. voltages of Correct polarity and magnitude to the two junctions of the transistor. this is nothing but biasing of the transistor. Because d.c. voltages are used are used to bias the transistor, biasing is known as d.c. biasing of the transistor.

Need for Biasing:

In transistor amplifier circuits, output signal power is always greater than i/p signal power. Now the question is how this amplification of power is achieved. The d.c. sources (d.c. biasing) supplies the power to the transistor circuit to get the output signal power greater than i/p signal power. thus we can say that the biasing is needed.

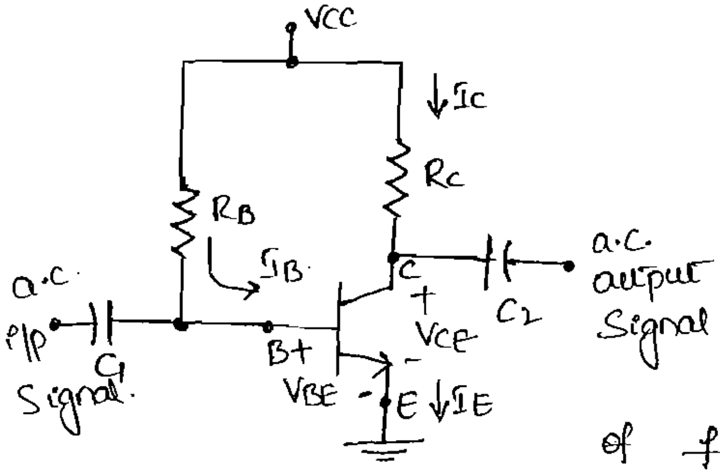
- to operate the transistor in the desired region
- to get the o/p signal power greater than i/p signal power.

Q point and Stability factor:

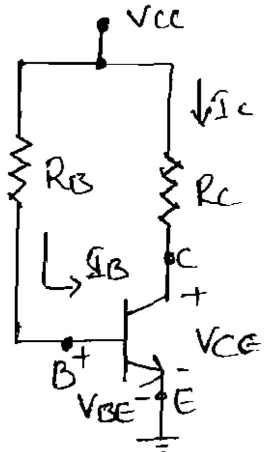
When we bias a transistor we Establish a certain current and voltage conditions for the transistor. these conditions are known as operating conditions (or) d.c. operating point (or) quiescent point.

The operating point must be stable for proper operation of the transistor However the operating point shifts with changes in transistor temperature dependent, the operating point also varies with changes in temperature. the stability factor indicates the degree of change in operating point due to variation in β, I_{CO} & V_{BE}

Fixed Bias Circuit:



The fig shows the fixed bias circuit. It is the simplest d.c. bias configuration. for the d.c. analysis we can replace capacitor with an open circuit because the reactance of the capacitor for d.c. is $X_C = 1/2\pi fC = \frac{1}{2\pi(0)C} = \infty$ the d.c equivalent of fixed bias circuit is shown below

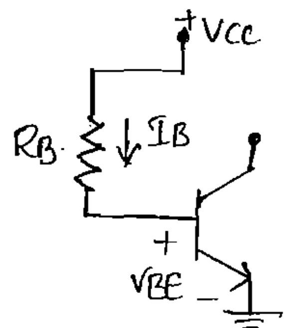


Base Circuit:

Applying kirchhoff's voltage law to the base circuit we get, $V_{CC} - I_B R_B - V_{BE} = 0$ so $I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow (1)$

consider the collector circuit, applying kirchhoff's law at the collector we get $V_{CC} - I_C R_C - V_{CE} = 0$

$\Rightarrow \quad V_{CE} = V_{CC} - I_C R_C \rightarrow (2)$



the magnitude of collector current is given by

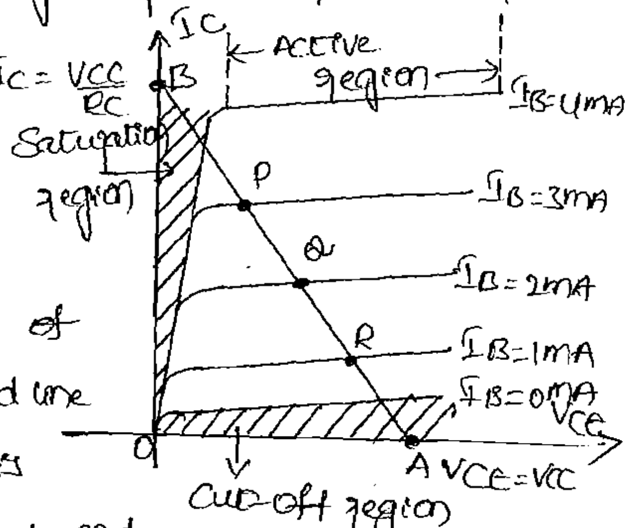
$I_C = \beta I_B$ & $I_C = \frac{V_{CC} - V_{CE}}{R_C}$

It is important to note that since the base current is controlled by the value of R_B and I_C is related to I_B by a constant β, the magnitude of I_C is not a function of R_C. changing R_C to any level will not effect the level of I_B (or) I_C as long as we remain in active region of the device. However the change in R_C will change the value of V_{CE}.

Load line and Quiescent point

D.C. load line: for fixed base circuit we have $I_C = \frac{V_{CC} - V_{CE}}{R_C}$

$I_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} V_{CE} = (-1/R_C) V_{CE} + \frac{V_{CC}}{R_C}$ By comparing this eq. with equation of straight line $y = mx + c$, m is slope of line, and 'c' is y-intercept on y-axis. we can draw a line on the graph of I_C verses V_{CE} which is having slope of "$-1/R_C$" and y-intercept of V_{CC}/R_C

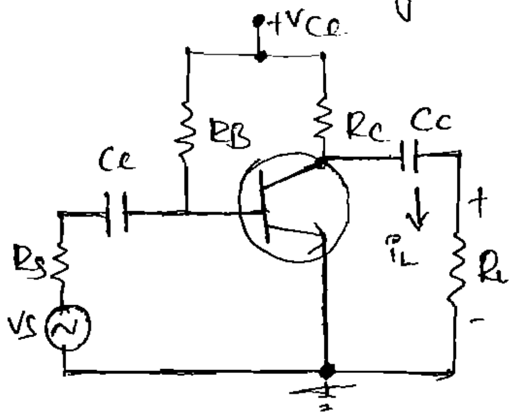


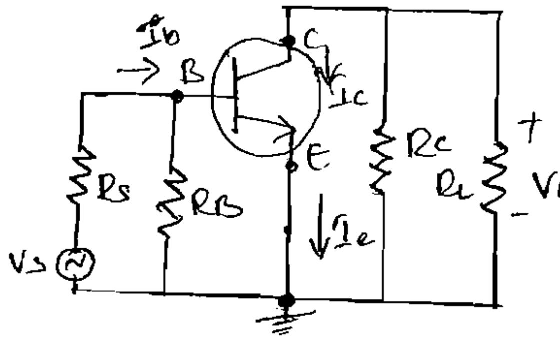
a) When $V_{CE} = V_{CC}$; $I_C = 0$, we get point A

When $V_{CE} = 0$; $I_C = \frac{V_{CC}}{R_C}$ we get 'B'

the fig shows the output characteristics of CE Configuration with points 'A' & 'B'. and line drawn b/w them, the line b/w A & B is called d.c. load line. the d.c. word indicates that only d.c. conditions are considered i.e. i/p signal is assumed to be zero. The d.c. load line is a plot of I_C vs V_{CE}, for a given value of R_C and a given level of V_{CC}. thus it represents all collector current levels and corresponding collector-emitter voltages that can exist in the ckt. knowing any one of I_C, I_B (or) V_{CE}, it is easy to determine the other two from load line. slope of d.c. load line depends on R_C. the intersection of curves of different values of I_B with d.c. load line gives different operating points. for different values of I_B, we have different intersection points. (quiescent point (or) Q point) such as P, Q and R

Coupling capacitors and by-pass capacitor acts as a short circuit. remember that capacitor blocks d.c. signal and passes a.c. signal. we replace d.c. source by a short cct, i.e. Vcc and ground lines.





The resulted a.c. equivalent circuit for the given CE amplifier is shown, from it, the collector cct resistance seen by the d.c. bias current I_{CQ} is $R_{dc} = R_c$. However it is appeared that collector signal current i_c sees a collector circuit resistance $R_{ac} = R_C \| R_L = \frac{R_C R_L}{R_C + R_L}$; since $R_{dc} \neq R_{ac}$, in general the concept of a.c. load line arises.

Applying KVL to the collector cct of the a.c. equivalent cct

$V_{ce} = I_c R_{ac}$ where. V_{ce} = a.c. collector to emitter voltage

I_c = a.c. collector current.

Since $I_c = i_c - I_{CQ}$ and $V_{ce} = V_{CEQ} - V_{CE}$

where i_c: total instantaneous collector current

V_{CE}: total instantaneous collector to emitter voltage.

so $V_{ce} = V_{CEQ} - V_{CE} = (i_c - I_{CQ}) R_{ac} \Rightarrow$

$$i_c = \frac{V_{CEQ}}{R_{ac}} - \frac{V_{CE}}{R_{ac}} + I_{CQ}.$$

All excursions of the a.c. signals I_c, and V_{ce} are represented by points on a.c. load line. if $i_c = I_{CQ}$ is substituted in above we find that $V_{CE} = V_{CEQ}$. This indicates that a.c. load line intersects d.c. load line at that point.

let find the points at which the ac load line intersects the axes of the o/p characteristics of CE configuration.

point a: by setting $i_C = 0$

$$\Rightarrow \quad V_{CEmax} = V_{CEQ} + I_{CQ} R_{ac} \longrightarrow (A)$$

point b: by setting $V_{CE} = 0$

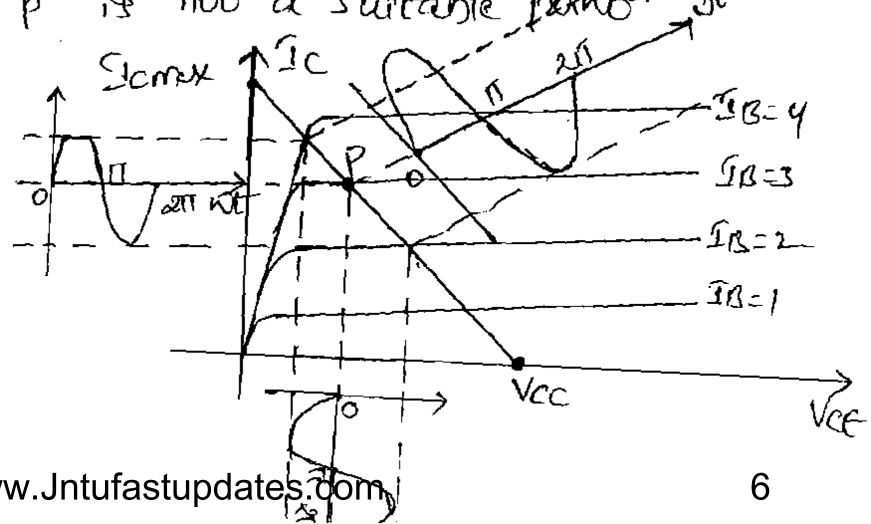
$$I_{Cmax} = \frac{V_{CEQ}}{R_{ac}} + I_{CQ} \longrightarrow (B)$$

Selection of operating point:

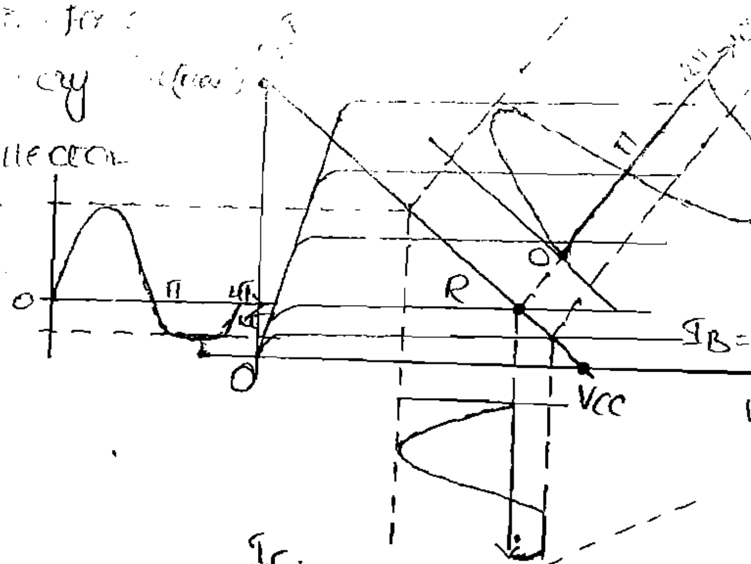
The operating point can be selected at different positions on d.c. load line, near saturation region, near cut-off region, (or) at the center. i.e. in active region. The selection of operating point will depends on it's application. When transistor is used as an amplifier, the Q point should be selected at the center of the d.c. load line to prevent any possible distortion in the amplified output signal.

Case1: Biasing circuit is designed to fix a Q point at P. let point P is very nearer to saturation region. The collector current is clipped at the +ve cycle, so eventhough base current varies sinusoidally, collector current is not a useful sinusoidal waveform. i.e. distortion is present at the o/p. so point P is not a suitable point.

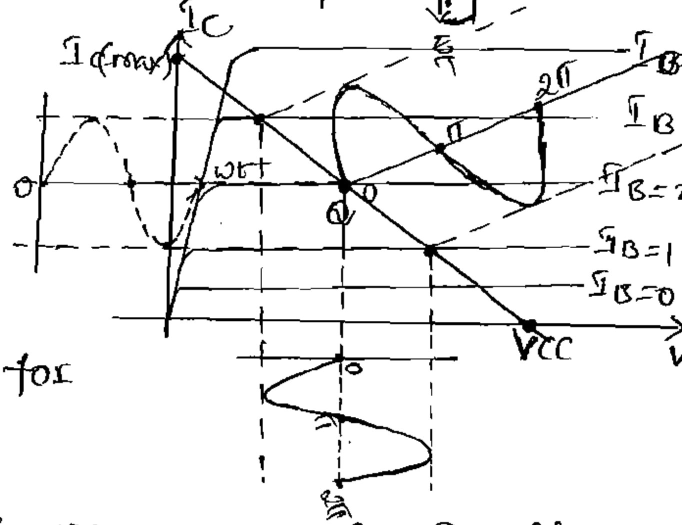
operating point near saturation point gives clipping at +ve peaks



a Q point at R. point R is very near to cut-off region. the collector current is clipped at -ve half cycle, so point R is also not suitable for operating point.



case 3: Biasing ckt is designed to fix a Q point at point Q. the o/p is sinusoidal waveform without any distortion. thus point Q is the best operating point.



Typical junction voltages & conditions for operating region

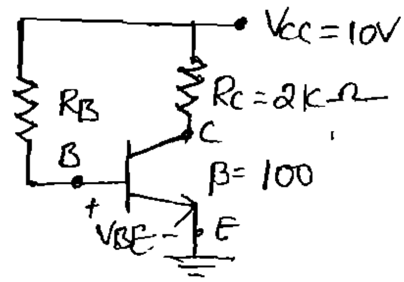
Below table shows the typical junction voltages for cut-off, active and saturation regions for n-p-n silicon and germanium transistors.

Transistor	$V_{CE(sat)}$	$V_{BE(sat)}$	$V_{BE(active)}$	$V_{BE(cut-in)}$	V_{BE} (cut-off)
Si	0.2	0.8	0.7	0.5	0V
Ge	0.1	0.3	0.2	0.1	-0.1V

To identify the operating region of transistor, we can observe certain conditions. they are

for saturation $I_B > \frac{I_C}{\beta_{dc}}$

for active region: $V_{CE} > V_{CE(sat)}$



In the shown ckt, for $R_B = 300k\Omega$, & $R_B = 150k\Omega$, cal. I_B, I_C and V_{CE} and determine region of operation.

Since Base-Emitter junction is not reverse biased, we can say that transistor is not cut-off region, let assume transistor is operating in active region.

Applying KVL around base loop we get

$V_{CC} = I_B R_B + V_{BE}$ Let ($V_{BE} = 0.7V$)

$V_{CC} = I_B \times 300 \times 10^3 + 0.7 = 10V$

$\Rightarrow I_B = \frac{9.3}{300 \times 10^{+3}} = 31 \mu A$

In active region $I_C = \beta I_B = 100 \times 31 \times 10^{-6} A = 3.1 mA$

Now by applying KVL around collector loop we get

$V_{CC} = I_C R_C + V_{CE}$

$10 = 3.1 \times 10^{-3} \times 2 \times 10^3 + V_{CE}$

$V_{CE} = 10 - 6.2 = 3.8V.$

$V_{CE} > V_{CE(sat)}$, collector to base junction is reverse biased and we can say that our assumption that transistor is in active region is justified.

Case 2: $R_B = 150K\Omega$

Since Base Emitter junction is not reverse biased hence transistor is not in cut-off region, and assume it is in active region, hence KVL around base is

$V_{CC} = I_B R_B + V_{BE} \Rightarrow I_B = \frac{10 - 0.7}{150 \times 10^3} = 62 \mu A$

In active region $I_C = \beta I_B \Rightarrow I_C = 6.2 mA$

KVL around collector

$V_{CC} = I_C R_C + V_{CE} \Rightarrow V_{CE} = 10 - 6.2 \times 10^{-3} \times 2 \times 10^3 = 10 - 12.4 = -2.4V$

It is important to note that collector voltage has to be zero (or) positive hence our assumption of transistor in active region is wrong. so it is in saturation

KVL around base loop

$V_{CC} = I_B R_B + V_{BE}(sat) \Rightarrow I_B = \frac{10 - 0.8}{150 \times 10^3} = 61.33\mu A$

Applying KVL around collector loop we get

$$V_{CC} = I_C R_C + V_{CE}(sat) \Rightarrow I_C = \frac{10-0.2}{2 \times 10^3} = 4.9mA.$$

to justify transistor in saturation $I_B > \frac{I_C}{\beta}$

$\Rightarrow \frac{I_C}{\beta} = \frac{4.9mA}{100} = 49\mu A$ so $(I_B = 61.33\mu A) > (49\mu A = \frac{I_C}{\beta})$ hence our assumption that transistor is in saturation is justified.

Stabilization against variations in I_{CO}, V_{BE} and β.

As we know that biasing circuit should be designed to fix the operating point (or) Q point at the center of active region But only fixing of operating point is not sufficient. while designing biasing circuit, care should be taken so that the operating point will not shift into an undesirable region. (i.e. cutoff (or) saturation region) designing the biasing ckt to stabilize the Q point is known as bias stability.

Two important factors that needs to be considered while design the biasing ckts which are responsible for shifting the operating point

i) Temperature ii) variation of h_{FE} (β) within manufactures tolerance

Temperature:

The change in temperature effect the following parameters of the transistor. i) I_{CO}, ii) V_{BE}, iii) β_{ac}

The flow of current in the circuit provides heat at the junx. This heat produces temperature at the junction. we know that minority carriers are temperature dependent. They increase with temperature, the increase in minority carriers increases leakage current I_{CEO}

$I_{CEO} = (1+\beta) I_{CBO}$

respectively. I_{CBO} doubles for every 10°C rise in temperature. Increase in I_{CEO} intum increases collector current

$I_C = \beta I_B + I_{CEO}$.

The increase in I_C further rises temperature at the collector junction and the same cycle repeats. The excessive increase in I_C shifts the operating point into the saturation region, changing the operating condition set by biasing ckt.

As the power dissipated with in a transistor is predominantly the power dissipated at its collector base junction, the power dissipation is given as $P_D = V_C I_C$. The increase in collector current increases the power dissipated at the collector junction. This in turn further increases temperature of the junction and hence increases the collector current. The process is cumulative. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called thermal runaway of the transistor. For any transistor max power dissipation is always a fixed value. This is known as max power dissipation rating of the transistor.

V_{BE}: V_{BE} changes with temperature at a rate of 2.5mV/°C. Base current I_B depends on V_{BE} and I_C depends on I_B, so I_C depends on V_{BE}; change of I_C changes the operating point.

β_{dc}: β_{dc} is also temperature dependent. As β_{dc} varies, I_C also varies, since $I_C = \beta I_B$. Change of collector current changes the operating point.

Therefore to avoid thermal instability, the biasing circuit should be designed to provide a degree of temperature stability i.e. Even though there are temperature changes, the changes in transistor parameters (V_{CEQ}, I_{CQ}, P_{Dmax}) should be very less so that the operating point shifting is minimum in the middle of active region.

Variation of hFE (β) with manufacturers tolerance

at the manufacturing side of the transistor, the value of β may get varied from transistor to transistor. the biasing circuit is designed according to the required β value. But due to change in β from unit to unit, the operating point may shift.

Requirements of a biasing circuit:

1) The emitter-base junction must be forward biased (0.6V to 0.7V) and collector-base junction must be reverse biased (with in max limits) i.e. transistor should be operated in middle of the active region (or) operating point (Q point) should be fixed at the center of the active region.

2) The circuit designed should provide a degree of temperature stability.

3) The operating point should be made independent of transistor parameters (such as β)

To maintain the operating point stable by keeping I_C and V_{CE} constants so that the transistor will always work in active region, the following techniques are normally used. i) Stabilization technique ii) Compensation techni

Stabilization techniques: Stabilization techniques refer to the use of resistive biasing circuits which allow I_B to vary so as to keep I_C relatively constant with variations in I_{CO}, β and V_{BE}.

Compensation techniques: These refer to the use of temperature-sensitive devices such as diodes, transistors, thermistors, etc. which provide compensating voltages and currents to maintain the operating point stable.

Stability factors:

Stability factor, which indicates degree of change in operating point due to variation in temperature. Since there are three variables which are temperature dependent, we can define 3 stability factors.

i) $S = \left.\dfrac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\ \beta \text{ Constant}}$ (or) $S = \left.\dfrac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\ \beta \text{ Constant}}$

ii) $S' = \left.\dfrac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}}$ (or) $S' = \left.\dfrac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}}$

iii) $S'' = \left.\dfrac{\partial I_C}{\partial \beta}\right|_{I_{CO},\ V_{BE} \text{ constant}}$ (or) $S'' = \left.\dfrac{\Delta I_C}{\Delta \beta}\right|_{I_{CO},\ V_{BE} \text{ Constant}}$

for a CE configuration, collector current is given as

$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1+\beta) I_{CBO}$$

when I_{CEO} changes by ΔI_{CBO}, I_B changes by ∂I_B and I_C changes by ∂I_C so

$$\partial I_C = \beta \partial I_B + (1+\beta)\partial I_{CBO}$$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta)\frac{\partial I_{CBO}}{\partial I_C} \Rightarrow$$

$$\frac{\partial I_{CBO}}{\partial I_C} = \frac{1-\beta\frac{\partial I_B}{\partial I_C}}{1+\beta} \Rightarrow S = \frac{1}{\frac{\partial I_{CBO}}{\partial I_C}} = \frac{1}{\frac{1-\beta\frac{\partial I_B}{\partial I_C}}{1+\beta}} = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

The general procedure to obtain stability factor for various biasing circuits is as follows.

Step1: obtain the expression for I_B.

Step2: obtain $\frac{\partial I_B}{\partial I_C}$ and use it in equation above to get S

Step3: In standard equation of I_C, replace I_B in terms of V_{BE} to get S'

Step4: differentiate the equation obtained in step3 w.r.t β' to get

Stability factor for fixed bias circuit:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \simeq \frac{V_{CC}}{R_B}.$$

When I_B changes by ∂I_B, V_{CC} and V_{BE} are uneffected.

$\therefore \frac{\partial I_B}{\partial I_C} = 0$ $\because I_C$ is not present in the equation

$$\Rightarrow S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)} = \frac{1+\beta}{1-0} = 1+\beta \Rightarrow \boxed{S = 1+\beta}$$

Stability factor S'

$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO}, \beta \text{ constants}}$; as we know $I_C = \beta I_B + (\beta+1) I_{CBO}$

now representing I_B interms of V_{BE} we get

$$I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) + (\beta+1) I_{CBO} = \beta \frac{V_{CC}}{R_B} - \beta \frac{V_{BE}}{R_B} + (\beta+1) I_{CBO}$$

$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \frac{\beta}{R_B} + 0 = \frac{-\beta}{R_B} \Rightarrow \boxed{S' = \frac{-\beta}{R_B}}$$

we know $S = 1+\beta$; $S' = -\beta/R_B$

$$\Rightarrow S' = \frac{-\beta(1+\beta)}{R_B(1+\beta)} \Rightarrow S' = \frac{-\beta S}{R_B(1+\beta)}$$

Stability factor S'' $\quad S'' = \frac{\partial I_C}{\partial \beta}\Big|_{V_{BE},\, I_{CO}\text{ constants}}$

as we know $I_C = \beta\frac{V_{CC}}{R_B} - \beta\frac{V_{BE}}{R_B} + (\beta+1)I_{CBO}$

$$\frac{\partial I_C}{\partial \beta} = \left(\frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B}\right) + I_{CBO} = I_B + I_{CBO} = \boxed{\frac{I_C}{\beta} = \frac{\partial I_C}{\partial \beta}}$$

since $\left\{ I_B = \frac{I_C}{\beta} \text{ and } I_B \gg I_{CBO} \right\}$

as we know $S = 1+\beta$; $\boxed{S'' = \frac{I_C}{\beta} = \frac{I_C(1+\beta)}{\beta(1+\beta)} = \frac{I_C S}{\beta(1+\beta)}}$

Different types of biasing circuits:

Different types of biasing circuits are

i) Fixed bias circuit

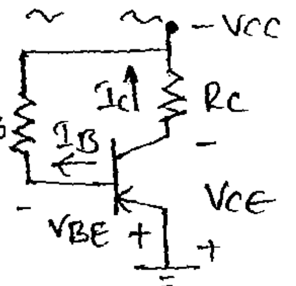
ii) collector to base bias circuit

iii) voltage divider / self bias circuit

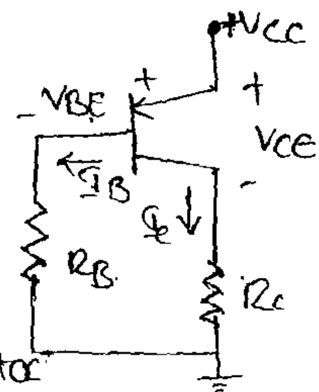
iv) Emitter stabilized bias circuit

v) Miscellaneous bias circuit

Fixed bias using a pnp transistor:



Fixed bias circuit using pnp transistor



Another way of drawing fixed bias circuit using pnp

Here the voltage polarities and current directions are reversed than that of npn transistor fixed bias circuit. However, the equations applied for the analysis of npn transistor fixed bias circuit can be applied for analysis of pnp transistor fixed bias circuit.

Advantages and Disadvantages of fixed bias ckt:

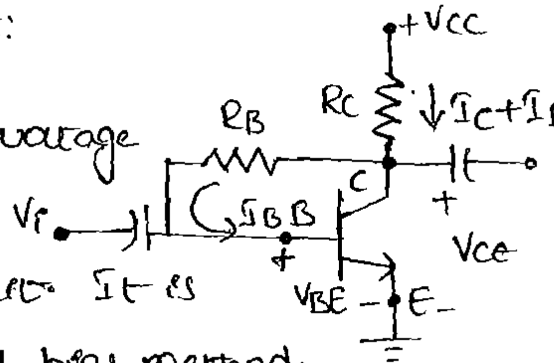
1) This is a simple circuit which uses very few components.

2) The operating point can be fixed anywhere on the active region of the characteristics by simply changing the value of R_B. Thus it provides max flexibility in the design.

3) This circuit does not provide any check on the collector current which increases with rise in temperature. i.e. thermal stability is not provided by this circuit. So operating point is not maintained. $I_C = \beta I_B + I_{CEO}$.

4) Since $I_C = \beta I_B$ and I_B is already fixed; I_C depends on β which changes unit to unit and shifts the operating point. So stabilization of operating point is very poor in fixed bias.

Collector to Base bias Circuit:



The fig shows dc. bias with voltage feed back also called collector to base bias circuit. It is an improvement over fixed bias method.

The biasing resistor is connected b/w collector and base of the transistor to provide a feed back path thus I_B flows through R_B and (I_C+I_B) flows through R_C

Circuit Analysis:

Applying KVL at base we get

$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE}$$

$$V_{CC} - V_{BE} = (1+\beta) I_B R_C + I_B R_B \qquad \beta >> 1$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_C} = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C}$$

Note that the only difference b/w the equation for I_C and that obtained for the fixed bias configuration is the term βR_C thus we can say that feed back path results in a reflection of the resistance R_C to the i/p circuit.

Applying Kirchhoff's law at the collector we get

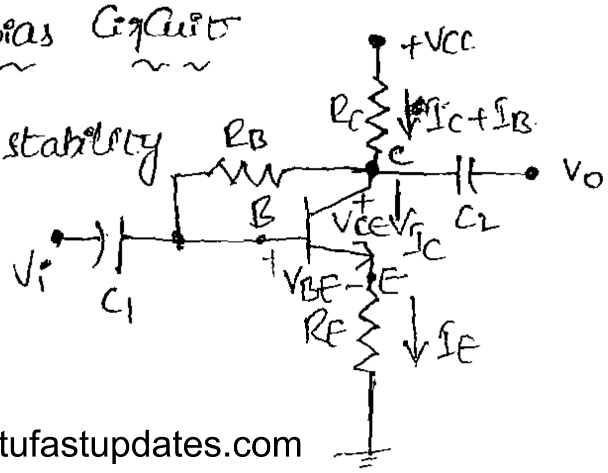
$$V_{CC} = (I_C + I_B)R_C + V_{CE} \Rightarrow V_{CE} = V_{CC} - (I_C + I_B)R_C$$

If there is a change in β due to piece to piece variation b/w transistor (or) if there is a change in β and I_{CO} due to change in temperature, then collector current I_C tends to increase, since $I_C = \beta I_B + I_{CEO}$ as a result voltage drop across R_C increases, since V_{CC} is constant, hence V_{CE} reduces, due to decrease in V_{CE}, I_B reduces, as I_C depends on I_B, decrease of I_B reduces original increase in I_C. The result is that the circuit tends to maintain a stable value of collector current, keeping the Q point fixed.

In this circuit, R_B appears directly across i/p (base) and output (collector). A part of the output is fed back to the i/p, and increase in collector current decreases the base current. Thus -ve feed back exist in the ckt. so this circuit is also called voltage feedback bias circuit.

Modified collector to base Bias Circuit

To further improve level of stability the Emitter resistance is connected as shown.



applying KVL to the base equation

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} - I_E R_E = 0.$$

$$V_{CC} - V_{BE} = (I_C + I_B) R_C + I_B R_B + (I_C + I_B) R_E$$

$$= (1+\beta) I_B (R_C + R_E) + I_B R_B.$$

$$= I_B (R_B + (1+\beta)(R_C + R_E))$$

$$\Rightarrow I_B = V_{CC} - V_{BE} \Big/ R_B + (1+\beta)(R_C+R_E) = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C+R_E)} \quad \because \beta > 1$$

Note that only difference b/w Equation for I_B and that obtained for fixed bias configuration is the term $\beta(R_C+R_E)$. thus we can say that the feed back path results in a reflection of the resistance R_C back to the i/p circuit, much like reflection of R_E. In general we can say that

$$I_B = \frac{V'}{R_B + \beta R'}$$

where $V' = V_{CC} - V_{BE}$

and $R' = 0$ for fixed bias

$R' = R_E$ for Emitter bias

$R' = R_C$ for Collector to base bias

$R' = R_C + R_E$ for collector to base bias with R_E.

at collector ckt

$$V_{CC} - (I_C + I_B) R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_E (R_C + R_E)$$

Stability factor for Collector to Base bias Circuit:

$$V_{CC} = I_C R_C + I_B (R_C + R_B) + V_{BE}$$

when I_{CBO} changes by ∂I_{CBO}, I_B changes by ∂I_B, and I_C changes by ∂I_C. There is no effect on V_{CC} & V_{BE} so

$$0 = \partial I_C R_C + \partial I_B (R_C + R_B) + 0 \Rightarrow \frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_C + R_B}$$

as we know

$$S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)} = \frac{1+\beta}{1+\beta \cdot \frac{R_C}{R_C+R_B}}$$

collector to base bias circuit is having lesser stability factor than for fixed bias circuit, hence this circuit provides better stability than fixed bias circuit.

Stabilization against change in β

The above equation shows that stability factor, S for the collector to base bias ckt also depends on β. If we design the circuit with condition $\beta R_C \gg R_B$ then we can make stability factor independent of β.

$$\text{as} \quad S = \frac{1+\beta}{1+\beta\frac{R_C}{R_C+R_B}} = \frac{(1+\beta)(R_C+R_B)}{R_C+R_B+\beta R_C} \simeq \frac{(1+\beta)(R_C+R_B)}{(1+\beta)R_C} = \frac{R_C+R_B}{R_C}$$

and also we know that

$$I_C = (1+\beta)I_{CBO} + \beta I_B \Rightarrow I_B = \frac{I_C - (1+\beta)I_{CO}}{\beta}$$

KVL at base of collector to base bias circuit

$$V_{CC} = (I_B+I_C)R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_B(R_C+R_B) + I_C R_C + V_{BE}$$

$$V_{CC} = \left[\frac{I_C - (1+\beta)I_{CO}}{\beta}\right](R_C+R_B) + I_C R_C + V_{BE}$$

$$\beta V_{CC} = I_C(R_C+R_B) - (1+\beta)I_{CO}(R_C+R_B) + \beta I_C R_C + \beta V_{BE}$$

$$\beta V_{CC} + (1+\beta)I_{CO}(R_C+R_B) - \beta V_{BE} = I_C(R_C+R_B+\beta R_C)$$

as $\beta \gg 1$, $\beta+1 \simeq \beta$.

$$I_C(R_B+\beta R_C) = \beta[V_{CC} - V_{BE} + I_{CO}(R_C+R_B)]$$

$$I_C \simeq \frac{V_{CC} - V_{BE} + I_{CO}(R_C+R_B)}{R_C} \quad \because \beta R_C \gg R_B.$$

from above we can say that, the collector current has become independent of β and hence stabilized against changes in β.

Stability factor S'

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\ \beta\ \text{constants}}.$$

Applying KVL, $V_{CC} = (R_B+R_C)I_B + I_C R_C + V_{BE}$

$I_B = V_{CC} - V_{BE} - I_C R_C \,/\, R_B+R_C$

$$\frac{I_C}{\beta} = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B} \Rightarrow \frac{I_C}{\beta} + \frac{I_C R_C}{R_C + R_B} = \frac{V_{CC} - V_{BE}}{R_C + R_B}$$

$$I_C \left[\frac{R_C + R_B + \beta R_C}{\beta (R_C + R_B)} \right] = \frac{V_{CC} - V_{BE}}{R_C + R_B} \Rightarrow I_C = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1+\beta) R_C}$$

$$\frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta) R_C} \Rightarrow S' = -\frac{\beta}{R_B + (1+\beta) R_C}$$

Relation b/w S and S'

we know $S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$ and $S' = \frac{-\beta}{R_B + (1+\beta) R_C}$

$$S = \frac{(1+\beta)(R_C + R_B)}{R_C + R_B + \beta R_C} = \frac{(1+\beta)(R_C + R_B)}{R_B + (1+\beta) R_C} \Rightarrow \frac{S}{(1+\beta)(R_C + R_B)} = -\frac{S'}{\beta}$$

$$\Rightarrow S' = \frac{-S\beta}{(1+\beta)(R_C + R_B)}$$; if S is small, S' is still smaller.

If we provide stability against I_{CO} variations, we get stability against V_{BE} variations also

Stability factor S'':

$$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\, V_{BE} \text{ constant}}$$

for collector to base bias circuit we have,

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = R_C (\beta I_B + I_B) + I_B R_B = I_B [R_B + (\beta+1) R_C]$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{(\beta+1) R_C + R_B} \Rightarrow I_C = \frac{\beta (V_{CC} - V_{BE})}{(1+\beta) R_C + R_B}$$

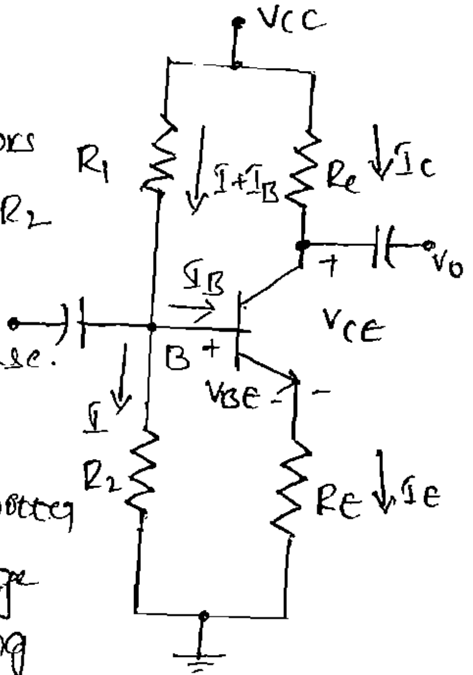
$$\frac{\partial I_C}{\partial \beta} = \frac{[(1+\beta) R_C + R_B][V_{CC} - V_{BE}] - \beta [V_{CC} - V_{BE}](R_C)}{[(1+\beta) R_C + R_B]^2}$$

$$= \frac{(V_{CC} - V_{BE})((1+\beta) R_C + R_B - \beta R_C)}{[(1+\beta) R_C + R_B]^2} = \frac{(V_{CC} - V_{BE})(R_C + R_B)}{[(1+\beta) R_C + R_B]^2}$$

$$\frac{(V \ldots)(R_B+R_C)}{[(1+\beta)R_C+R_B][R_B+(1+\beta)R_C]} \qquad \frac{I_C}{\beta} \times \frac{(R_B+R_C)}{((1+\beta)R_C+R_B)}$$

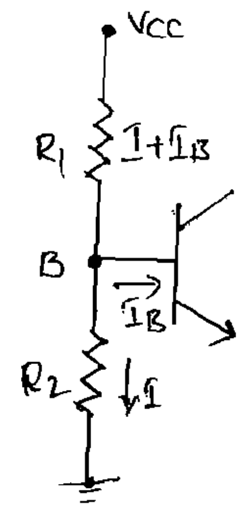
as we know $S'' = \dfrac{I_C\,(R_B+R_C)}{\beta[(1+\beta)R_C+R_B]} = \boxed{\dfrac{I_C}{\beta}\,\dfrac{S}{(1+\beta)} = S''}$

Voltage divider bias / self bias circuit



The biasing is provided by three resistors R_1, R_2, and R_E. The resistors R_1 and R_2 acts as potential divider giving a fixed value to point B which is Base. If collector increases due to change in temperature (or) change in β the emitter current I_E also increases. and voltage drop across R_E increases, reducing voltage difference b/w base & emitter (V_{BE}). due to reduction in V_{BE}, base current I_B hence collector current I_C also reduces. so therefore we say that −ve feed back exists in the emitter bias circuit. this reduction in collector current I_C compensates for original change in I_C

Circuit Analysis:



voltage across R_2 is the base voltage V_B.
Applying the voltage divider theorem to find V_B, we get

$$V_B = \frac{R_2 I}{R_1(I+I_B)+R_2(I)} \times V_{CC}$$

as $I \gg I_B$ $\quad V_B = \dfrac{R_2}{R_1+R_2} \times V_{CC}$

applying KVL at collector circuit we get

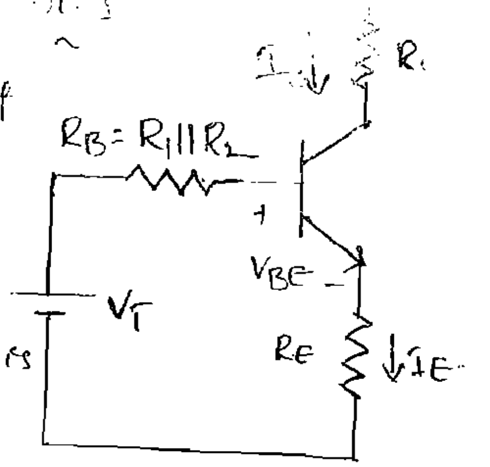
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0.$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \;; \quad V_E = I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

Simplified circuit of voltage divider bias

The circuit shows simplified circuit of voltage divider bias. Here R_1 and R_2 are replaced by R_B and V_T, where R_B is the parallel combination of R_1 & R_2 and V_T is the thevenin's voltage. R_B is



Thevenin's equivalent circuit for voltage

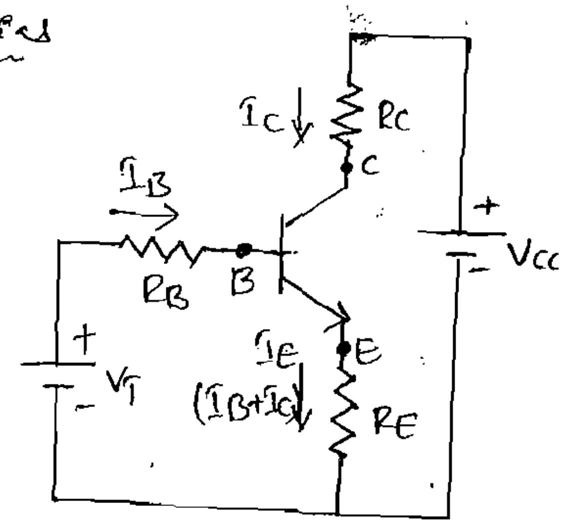
$R_B = \frac{R_1 R_2}{R_1+R_2}$; KVL at base of the ckt is $V_T = I_B R_B + V_{BE} + I_E R_E$

$$V_T = I_B R_B + I_B R_E + I_C R_E + V_{BE}$$

$$\Rightarrow V_{BE} = V_T - (R_B + R_E) I_B - I_C R_E$$

Stability factor for voltage divider Bias

Here $V_T = \frac{R_2 \times V_{CC}}{R_1 + R_2}$; $R_B = \frac{R_1 R_2}{R_1 + R_2}$



at base circuit we have

$$V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

differentiating w.r.t I_C and considering V_{BE} to be independent of I_C, we get

$$0 = \frac{\partial I_B}{\partial I_C} R_B + \frac{\partial I_B}{\partial I_C} R_E + R_E \Rightarrow \frac{\partial I_B}{\partial I_C} = -R_E / R_B + R_E$$

as we know $S = \frac{1+\beta}{1 - \beta \frac{\partial I_B}{\partial I_C}} = \frac{1+\beta}{1 + \beta \frac{R_E}{R_B + R_E}} = \frac{1+\beta (R_B + R_E)}{R_B + (1+\beta) R_E}$

$$S = (1+\beta)(1 + R_B/R_E) \Big/ (1+\beta) + \frac{R_B}{R_E}$$

the ratio of R_B/R_E controls the value of stability factors.

If $R_B/R_E \ll 1$ then $S = \frac{(1+\beta)}{(1+\beta)} = 1$ practically $R_B/R_E \neq 0$ but to have better stability factor's we have to keep ratio of R_B/R_E as small as possible.

2) To keep R_B/R_E small, it is necessary to keep R_B small, this means that $R_1 \| R_2$ must be small. Due to [illegible] small values of R_1 & R_2, potential divider circuit will draw more current from V_{CC} reducing life of battery. So while designing it we make R_2 much smaller than R_1 then parallel combination results small R_B without drawing more current through V_{CC}. Reducing R_B will reduce i/p impedance of the circuit, since R_B comes in parallel with i/p. This is not desirable in Amplifier circuits hence R_B cannot be made very small.

3) Emitter resistance R_E is the another parameter, uses to decrease ratio of R_B/R_E, by increasing R_E. But as we increase R_E, drop $I_E R_E$ will also increase and since V_{CC} is constant; drop across R_C will reduce. This shifts the operating point Q which is not desirable hence there is limit of increasing of R_E.

So the compromising values are

S - Small, $R_B \rightarrow$ Reasonably small, $R_E \rightarrow$ Not very large.

4. If ratio of R_B/R_E is fixed, S increases with β. So stability decreases with increasing β. S is essentially independent of β for small values of S.

Stability factor S'

Stability factor S' is given by

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\, \beta \text{ constant}}$$

we know that

$$I_C = (1+\beta) I_{CO} + \beta I_B$$

and $V_T = I_B R_B + V_{BE} + (I_B + I_C) R_E$

$$\Rightarrow V_{BE} = V_T - (R_E + R_B) I_B - R_E I_C$$

from (1) $I_B = I_C - (1+\beta) I_{CO} / \beta$

Substituting I_B, we get

$$V_{BE} = V_T - (R_E+R_B)\left[\frac{I_C - (1+\beta)I_{CO}}{\beta}\right] - R_E I_C$$

$$= V_T - \frac{(R_E+R_B)I_C}{\beta} + \frac{(1+\beta)(R_E+R_B)}{\beta} I_{CO} - R_E I_C$$

$$= V_T - \left[\frac{(1+\beta)R_E + R_B}{\beta}\right] I_C + \frac{(R_E+R_B)(1+\beta)}{\beta} I_{CO}.$$

differentiating above equation w.r.t V_{BE} with I_{CO} and β constant, we get

$$1 = 0 - \frac{(1+\beta)R_E + R_B}{\beta}\frac{\partial I_C}{\partial V_{BE}} \Rightarrow \frac{\partial I_C}{\partial V_{BE}} = -\beta / R_B + (1+\beta)R_E$$

$$\Rightarrow S' = -\beta / R_B + (1+\beta)R_E$$

Relation between S and S'

we know that

$$S = (1+\beta)\frac{1 + R_B/R_E}{1+\beta+R_B/R_E} = \frac{(1+\beta)(R_E+R_B)}{(1+\beta)R_E + R_B}$$

$$\Rightarrow \frac{S}{(1+\beta)(R_E+R_B)} = \frac{1}{R_B + (1+\beta)R_E}$$

$$\Rightarrow S' = -\beta \times \frac{S}{(1+\beta)(R_E+R_B)} = -\frac{S}{(R_E+R_B)} \times \frac{\beta}{1+\beta}.$$

if value of 'S' is lower, leads to lowering value of S'. Thus as we reduce 'S' towards unity, we minimise the change of I_C with respect to both, V_{BE} and I_{CO}.

Stability factor S''

S'' is given by $S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO}, V_{BE}\text{ constant}}$

we know that $V_{BE} = V_T - \frac{[R_B + (1+\beta)R_E]}{\beta} I_C + \left[\frac{(R_E+R_B)(1+\beta)}{\beta}\right] I_{CO}.$

$$V_{BE} = V_T - \frac{R_B + (1+\beta)R_E}{\beta} I_C + V'$$

$$V' = \frac{(R_B+R_E)(1+\beta)}{\beta} I_{CO} \simeq (R_B+R_E) I_{CO} \quad \because \beta >> 1$$

$\Rightarrow I_C = \beta(V_T + V' - V_{BE}) / R_B + R_E(1+\beta)$

differentiating above equation w.r.t β and V' independent of β we get

$$\frac{\partial I_C}{\partial \beta} = [R_B + R_E(1+\beta)][V_T + V' - V_{BE}] - \beta[V_T + V' - V_{BE}]R_E / [R_B + R_E(1+\beta)]^2$$

$$= \frac{(V_T + V' - V_{BE})[R_B + R_E] \times (1+\beta)}{(1+\beta)[R_B + R_E(1+\beta)][R_B + R_E(1+\beta)]} = \frac{S[V_T + V' - V_{BE}]}{(1+\beta)[R_B + R_E(1+\beta)]}$$

Since $S = (1+\beta)(R_E + R_B) / R_B + (1+\beta)R_E$

$$\frac{\partial I_C}{\partial \beta} = \beta S(V_T + V' - V_{BE}) / \beta(1+\beta)(R_B + R_E(1+\beta)) = \frac{I_C S}{\beta(1+\beta)}$$

Since $I_C = \beta(V_T + V' - V_{BE}) / [R_B + R_E(1+\beta)]$

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C S}{\beta(1+\beta)}$$

Thus, the change in collector current due to change in β is

$$\partial I_C = S'' \partial \beta = \frac{I_C S}{\beta(1+\beta)} \partial \beta.$$

where $\partial \beta = \beta_2 - \beta_1$ may represents a large change in β. Hence it is not clear weather to use β_1, β_2, S'' is obtained by taking finite differences rather than by evaluating a derivative

thus $S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_{C2} - I_{C1}}{\beta_2 - \beta_1}$; we know that $I_C = \frac{\beta(V_T + V' - V_{BE})}{R_B + R_E(1+\beta)}$

$$\frac{I_{C2}}{I_{C1}} = \frac{\beta_2[R_B + R_E(1+\beta_1)]}{\beta_1[R_B + R_E(1+\beta_2)]} \Rightarrow$$

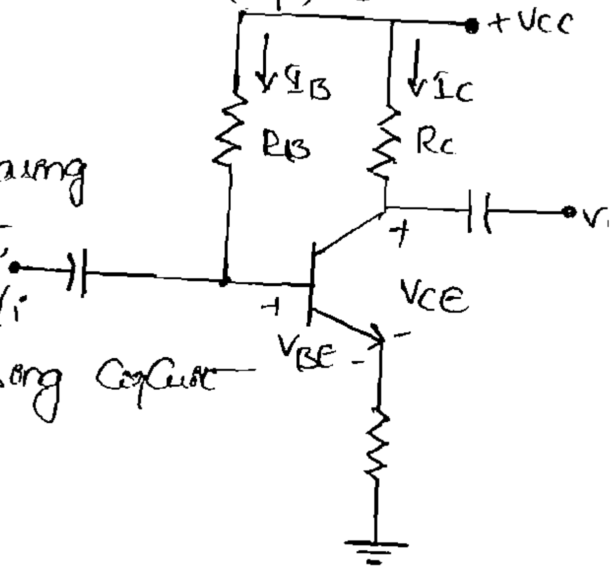
$$\frac{I_{C2} - I_{C1}}{I_{C1}} = \frac{\beta_2[R_B + R_E(1+\beta_1)] - \beta_1[R_B + R_E(1+\beta_2)]}{\beta_1[R_B + R_E(1+\beta_2)]}$$

$$\frac{\partial I_C}{I_{C1}} = \frac{\beta_2 R_B + \beta_2 R_E + \beta_1\beta_2 R_E - \beta_1 R_B + \beta_1 R_E - \beta_1\beta_2 R_E}{\beta_1[R_B + R_E(1+\beta_2)]}$$

$$= \frac{\beta_2 - \beta_1}{\beta_1} \frac{(R_B + R_E)}{R_B + R_E(1+\beta_2)} = \frac{\partial \beta}{\beta_1} \frac{R_B + R_E}{R_B + R_E(1+\beta_2)}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{I_{C1}}{\beta_1} \cdot \frac{R_B + R_E}{R_B + R_E(1+\beta_2)} = \frac{(1+\beta)(R_B+R_E)}{R_B+R_E(1+\beta_2)} \times \frac{I_{C1}}{\beta_1}$$

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_{C1}}{\beta_1} \times \frac{S_2}{(1+\beta_2)} \quad \text{since } S_1 = S = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E}$$



Emitter stabilized bias circuit:

To improve the stability of the biasing circuit over the fixed bias circuit, the emitter resistance is connected in the biasing circuit. Such biasing circuit is known as Emitter bias circuit.

Circuit Analysis:

Applying KVL at the base of the circuit, we get

$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$; we know that $I_E = (1+\beta) I_B$.

$\Rightarrow V_{CC} - V_{BE} = I_B R_B + (1+\beta) I_B R_E \Rightarrow I_B = V_{CC} - V_{BE} / R_B + (1+\beta) R_E$

as $\beta >> 1$

$\Rightarrow I_B = V_{CC} - V_{BE} \,|\, R_B + \beta R_E$

Note that the only difference b/w the equation for I_B and that obtained for the fixed bias configuration is the term βR_E

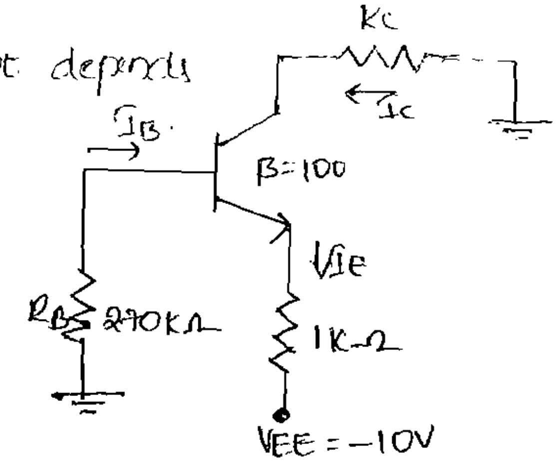
Applying KVL at collector circuit we get

$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0 \Rightarrow$

$V_C = V_{CC} - I_C R_C$; $V_E = I_E R_E$; $V_{CE} = V_C - V_E$

The addition of the emitter resistance, R_E in the emitter bias circuit provides improved stability, i.e. the ~~bias~~ d.c. bias currents and voltages remains closer to where they were set by the circuit against the changes in temperature and transistor β.

Miscellaneous bias configuration



In this biasing, the biasing doesnot depends on basic biasing configurations.

as emitter base junction is forward biased assume transistor is in active region

Applying KVL at base we get

$-V_{EE} = I_B R_B + V_{BEact} + I_E R_E$

$\Rightarrow \quad 10 = I_B R_B + V_{BEact} + (1+\beta) I_B R_E \Rightarrow 10-0.7 = 270\times10^3 I_B + 101\times10^3 I_B$

$\Rightarrow \quad 9.3 = 371\times10^3 I_B \Rightarrow I_B = \frac{9.3}{371\times10^3} = 25.067\mu A$

Applying KVL at collector we get

$-V_{EE} = I_C R_C + V_{CEact} + I_E R_E$

$= \beta I_B R_C + V_{CEact} + (1+\beta) I_B R_E$

$10 = 100\times25.067\times10^{-6}\times10^3 + V_{CEact} + (1+100)\times25.067\times10^{-6}\times10^3$

$\Rightarrow V_{CE(act)} = 4.961\,V$

and $I_C = \beta I_B = 100\times25.067\times10^{-6} = 2.5067\,mA$

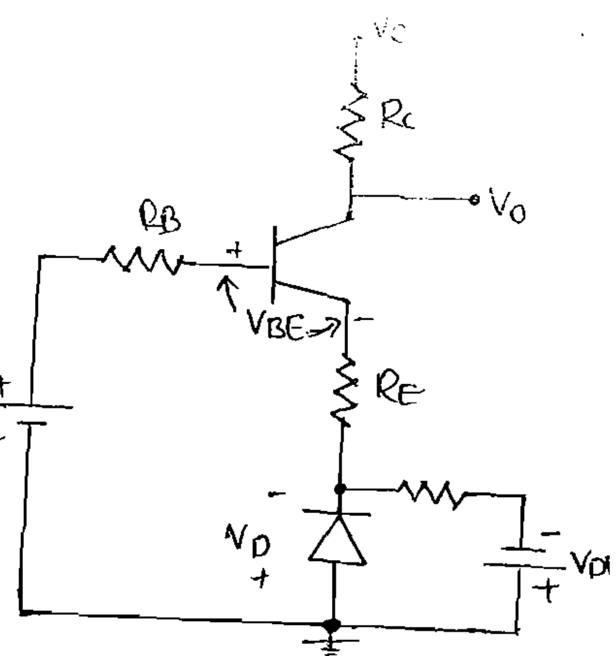
Bias compensation using diodes and transistors:

The biasing circuits so far discussed provide stability of operating point in case of variations in the transistor parameters such as I_{CO}, V_{BE} and β. the collector to base bias and the voltage follower bias use the -ve feed back to do the stabilization action. this -ve feed back reduces the amplification of the signal. If this loss in signal amplification is intolerable and extremely stable biasing conditions are required, then it is necessary to use compensation techniques. these use temperature sensitive devices such as diodes, transistors, thermistors. etc.

Diode compensation technique

Compensation for V_{BE}:

a) Diode in Emitter Circuit:



The circuit shows the voltage divider bias. With bias compensation technique. Here separate supply V_{DD} is used to keep diode in forward biased condition. If the diode used in the circuit is of same material and the type as transistor, the voltage across the diode will have same temperature coefficient ($-2.5mV/°c$) as the base to emitter voltage V_{BE}. So when V_{BE} changes by ∂V_{BE} with changes in temperature, V_D changes by ∂V_D and $\partial V_D' \approx \partial V_{BE}$, the changes tend to cancel each other.

Applying KVL to the base region

$$V_T = I_B R_B + V_{BE} + (I_C + I_B) R_E - V_D.$$

$$= I_B (R_B + R_E) + V_{BE} + I_C R_E - V_D$$

by considering leakage current we have

$$I_C = \beta I_B + (1+\beta) I_{CO} \Rightarrow I_B = \frac{I_C}{\beta} + \frac{(1+\beta) I_{CO}}{\beta}$$

$$V_T = \left[\frac{I_C}{\beta} + \frac{(1+\beta)}{\beta} I_{CO}\right](R_B + R_E) + I_C R_E + V_{BE} - V_D$$

$$= \frac{I_C}{\beta}[(R_B + R_E)] + \frac{\beta I_C R_E}{\beta} + \frac{(1+\beta)}{\beta} I_{CO} (R_B + R_E) + V_{BE} - V_D.$$

$$= \frac{I_C}{\beta}[R_B + (1+\beta) R_E] + \frac{(R_B + R_E)(1+\beta) I_{CO}}{\beta} + V_{BE} - V_D$$

$$\Rightarrow I_C = \frac{\beta[V_T - (V_{BE} - V_D)] + (R_B + R_E)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E}$$

Since V_D traces V_{BE} with respect to temperature, it is clear that I_C will be insensitive to variations in V_{BE}

[illegible]

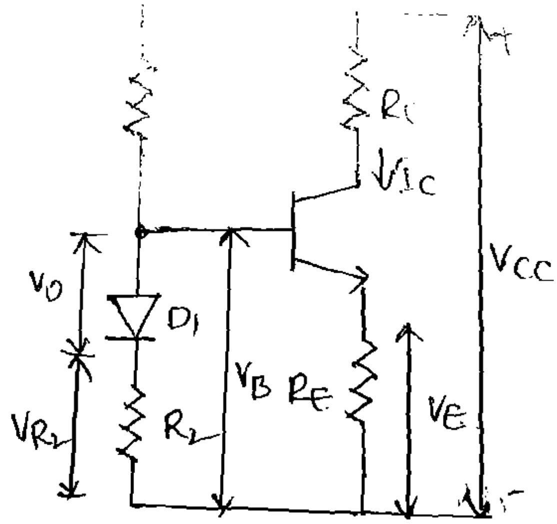


fig. shows diode compensation technique used in voltage divider bias. Here, diode is connected in series with R_2 in voltage divider circuit and it is forward biased condition.

we know that $I_E = \frac{V_B - V_{BE}}{R_E} = \frac{V_E}{R_E}$ Since $I_C \cong I_E$

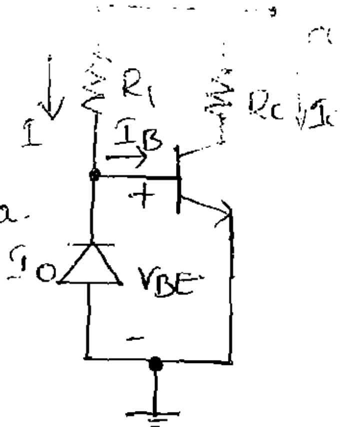
$$\Rightarrow I_C \approx I_E = \frac{V_B - V_{BE}}{R_E}$$

When V_{BE} changes with temperature, I_C also changes. To cancel the change in I_C, one diode is used in this circuit for compensation. the voltage at V_B is given as

$$V_B = V_{R_2} + V_D \; ; \Rightarrow I_C \cong I_E = \frac{V_{R_2} + V_D - V_{BE}}{R_E}$$

if the diode which is used in this circuit is of same material and type as transistor, the voltage across the diode will have same temperature coefficient ($-2.5mV/^{\circ}C$) as the base to emitter voltage V_{BE}. so when V_{BE} changes by ∂V_{BE} with change in temperature, V_D changes by ∂V_D and $\partial V_D = \partial V_{BE}$ the changes tend to cancel each other and leave the collector current as $I_C = \frac{V_{R_2}}{R_E}$ which is uneffected due to change in V_{BE}. from fig. we can see that biasing is provided by R_1, R_2 and R_E. The changes in V_{BE} due to temperature are compensated by changes in diode voltage which keeps I_C stable at Q point

Compensation of I_{CO}



In case of Ge transistors, changes in I_{CO} with temperature are comparatively larger than Silicon transistor. Hence in Ge changes of I_{CO} with temperature play a vital role in collector current stability than changes in V_{BE}. The diode is kept in reverse bias, the diode has the only leakage current. If the diode and the transistor are of same type and material, the leakage current I_0, will increase with temperature at the same rate as the collector leakage current

from above fig $I = \frac{V_{CC} - V_{BE}}{R_1}$; $I = I_B + I_0 \Rightarrow I_B = I - I_0$

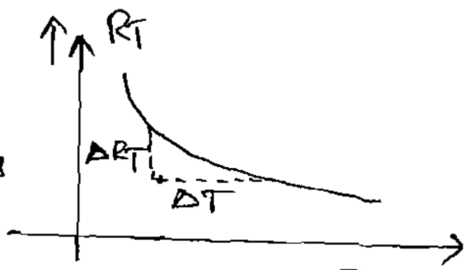
for 'Ge', $V_{BE} = 0.2V$ which is very small, and neglecting change on V_{BE} with temperature we can write

$I = V_{CC}/R_1 \simeq$ Constant; we know that $I_C = \beta I_B + (1+\beta) I_{CO}$.

$\Rightarrow I_C = \beta I - \beta I_0 + (1+\beta) I_{CO}$ $\beta >> 1 \Rightarrow I_C = \beta I - \beta I_0 + \beta I_{CO}$.

If $I_0 = I_{CO} \Rightarrow I_C = \beta I$; As I is constant, I_C remains fairly constant $\Rightarrow$ changes by I_{CO} with temperature are compensated by diode and collector current remains fairly constant.

Thermistor Compensation:

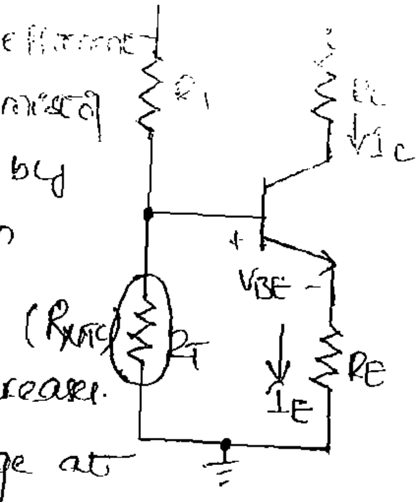


The method of transistor compensation uses temperature sensitive elements, thermistors rather than diodes (or) transistors. It has a negative temperature coefficient, its resistance decreases exponentially with increasing temperature

Temperature Vs R_T resistance of thermistor

slope of the curve $= \frac{\partial R_T}{\partial T}$ [temperature coefficient for thermistor]

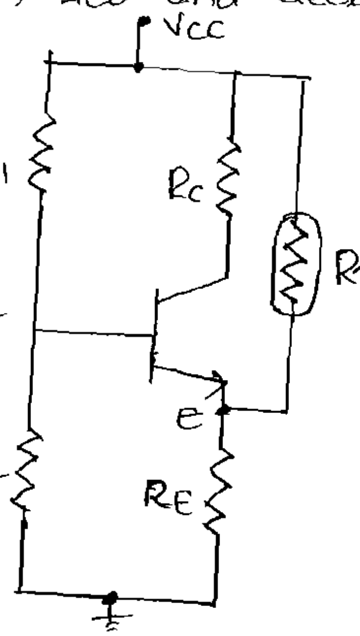
The thermistor has a -ve temperature coefficient of resistance. The next fig shows thermistor compensation technique; R_1 is replaced by thermistor R_T in self bias circuit. With increase in temperature, R_T decreases. Hence voltage drop across it also decreases. This voltage is nothing but the voltage at the base w.r.t ground. Hence V_{BE} decreases which reduces I_B. This behaviour will tend to offset the increase in collector current with temperature.



hence $I_C = \beta I_B + (1+\beta) I_{CO}$.

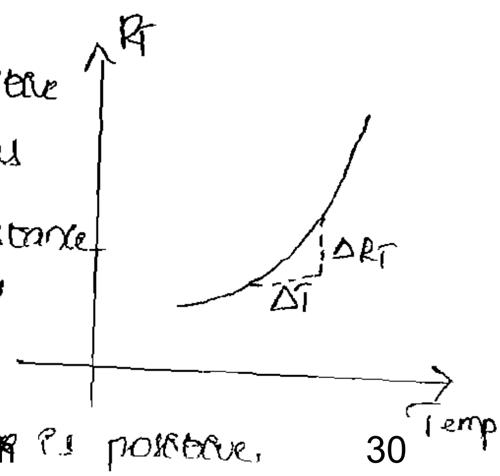
In above equation, there is increase in I_{CO} and decrease in I_B which keeps I_C almost constant.

The next fig shows another transistor compensation technique. +ve thermistor is connected b/w emitter and V_{CC} to minimize the increase in collector current due to changes in I_{CO}, V_{BE} (or) β. With temperature I_C increases with temperature and R_T decreases with increase of temperature so current flowing through R_E increases. E-B junction is forward biased, hence V_{BE} reduces, so base current reduces.



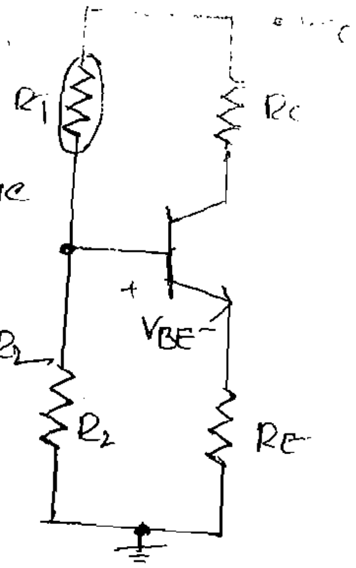
Sensistor compensation technique:

This technique uses temperature sensitive resistive element, sensistor, which has +ve temperature coefficient, its resistance increases exponentially with increase of temperature.



slope of curve $= \frac{\partial R_T}{\partial T}$ slope is positive.

The fig shows sensistor compensation technique.



R_T and R_2 forms the resistors of potential divider network. With increase of temperature R_T also increases which decrease current flowing through it. Hence current through R_2 decreases which decreases voltage at R_2 i.e. V_{BE}, hence I_B decreases, and hence I_C remains fairly constant.

Thermal runaway:

The max avg. power $P_{D(max)}$ which a transistor can dissipate depends up on the transistor construction and lie in the range of few milliwatts to 200 W as mentioned earlier. The power dissipated with in a transistor is predominantly the power dissipated at the collector base junction. Thus max power is limited by the temperature that the collector base junction can withstand. For Si it is range of 150 to 200°C, for Ge 60° to 100°C. The collector base junction temperature may rise because of two reasons. i) Due to rise in ambient temperature

ii) Due to self heating.

The increase in the collector current increases the power dissipated at the collector junction. This, in turn further increases the temperature of the junction and hence increase in collector current. The process is cumulative and it is referred to as a self heating. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called thermal runaway of the transistor.

It is necessary to avoid thermal runaway which may even burn and destroy transistor. To avoid thermal runaway, the rate at which heat is released at the collector junction must not exceed the rate at which heat can be dissipated.

The temperature rise at collector junction is proportional to the power dissipated at the junction.

$\Delta T = T_J - T_A = \theta P_D$; $T_J \to$ junction temperature in °C

$T_A \to$ Ambient temperature in °C. $P_D \to$ power dissipation at collector junction.

$\theta \to$ constant of proportionality.

$\theta \to$ also referred as thermal resistance.

$\theta = T_J - T_A / P_D$; unit of θ is °C/watt.

the maximum collector power P_C allowed for safe operation is specified at 25°C

to avoid thermal run away $\frac{\partial P_C}{\partial T_J} < \frac{\partial P_D}{\partial T_J}$

as we know $T_J - T_A = \theta P_D \Rightarrow 1 = \theta \cdot \frac{\partial P_D}{\partial T_J}$

$\Rightarrow \frac{\partial P_D}{\partial T_J} = 1/\theta \Rightarrow \frac{\partial P_C}{\partial T_J} < \frac{1}{\theta}$

By properly designing a biasing ckt it is possible to ensure that transistor cannot runaway below a specified ambient temperature (or) even under any condition.

for voltage divider bias ckt

P_C = heat generated at collector junction

= d.c. power i/p to the ckt − power loss as I^2R in R_C & R_E

$P_C = V_{CC} I_C - I_C^2 R_C - I_E^2 R_E$; as $I_C \simeq I_E$

so $P_C = V_{CC} I_C - I_C^2 (R_C + R_E)$

$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C(R_C+R_E)$, as we know $\frac{\partial P_C}{\partial I_C} \cdot \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta}$

$\frac{\partial I_C}{\partial T_j}$ can be written as $= S\frac{\partial I_{CO}}{\partial T_j} + S'\frac{\partial V_{BE}}{\partial T_j} + S''\frac{\partial \beta}{\partial T_j}$ since junction temperature affects collector current by affecting I_{CO}, V_{BE} and β but as we are doing analysis for thermal runaway, I_{CO} dominates. so $\frac{\partial I_C}{\partial T_j} = \frac{\partial I_{CO}}{\partial T_j}$

As reverse saturation current for both 'Si' & 'Ge' increases about %7 per °C rise, we get $\frac{\partial I_{CO}}{\partial T_j} = 0.07 I_{CO}$.

$\Rightarrow \frac{\partial I_C}{\partial T_j} = S \times 0.07 I_{CO} \Rightarrow [V_{CC} - 2I_C(R_C+R_E)]\, S(0.07 I_{CO}) < \frac{1}{\theta}$

as S, I_{CO} and θ ~~are~~ positive, to satisfy above eq.

$V_{CC} < 2I_C(R_C+R_E) \Rightarrow \frac{V_{CC}}{2} < I_C(R_C+R_E)$

Applying KVL to the collector circuit of voltage divider bias configuration we get

$V_{CE} = V_{CC} - I_C(R_E+R_C) \quad \because I_C \cong I_E$

$\Rightarrow I_C(R_E+R_C) = V_{CC} - V_{CE} \Rightarrow \frac{V_{CC}}{2} < V_{CC} - V_{CE} \Rightarrow V_{CE} < \frac{V_{CC}}{2}$

Thus if $V_{CE} < \frac{V_{CC}}{2}$, the stability is ensured. but in transformer coupled circuits, R_C & R_E are small hence $V_{CE} \cong V_{CC}$. so it is necessary to design transformer coupled circuits with stability factor as close to 1 as possible to avoid thermal runaway

FET biasing

In FET's as temperature increases drain resistance also increases, so that reduction of drain current takes places. However, the wide differences in maximum and minimum transfer characteristics make it necessary to keep drain current I_D stable at FET's quiescent value.

as we know $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

different biasing circuits of FET are

i) Fixed bias circuit ii) Self bias circuit iii) voltage divider bias

The below fig shows fixed bias circuit which is simplest a seperate supply V_{GG} is connected such that gate is more negative than source. the current through R_G is $I_G = 0$.

S1: calculate V_{GS}:

for d.c. analyses $I_G = 0A \Rightarrow V_{GS} = -V_{GG}$

since V_{GG} is fixed in magnitude, hence the voltage V_{GS} is also fixed.

S2: Calculate I_{DQ}:

I_D can be calculated by using

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

S3) calculate V_{DS}:

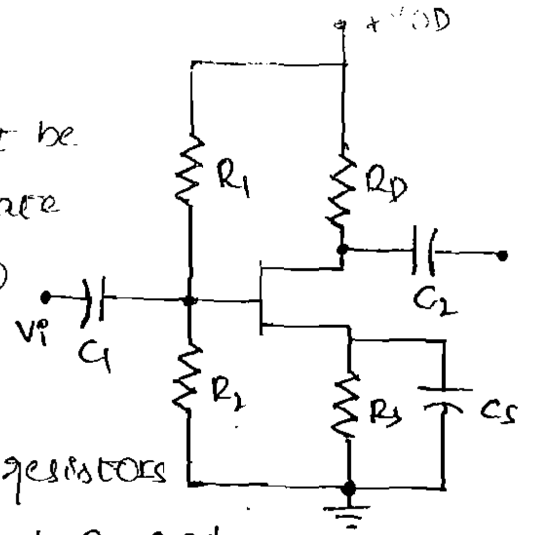
By KVL at drain, we get

$$V_{DD} - I_D R_D - V_{DSQ} = 0$$

$$\Rightarrow V_{DSQ} = V_{DD} - I_D R_D$$

The main draw back of fixed bias ckt is it requires two power supplies.

Voltage divider Bias Circuit



The voltage at the source of the JFET must be more positive than the voltage at the gate inorder to keep the gate-source junction reverse biased. the source voltage is

$V_s = I_D R_s$.

The gate voltage is set by resistors R_1 and R_2. Coupling capacitors C_1 and C_2 and source resistor R_s, bypass capacitor C_s are assumed to be open circuit for D.C analysis.

D.C. analysis:

S1: Calculate $V_G = \frac{V_{DD} R_2}{R_1+R_2}$ $\because I_G = 0$.

S2: obtain Expression for V_{GS}.

Applying KVL to the i/p ckt we get

$V_G - V_{GS} - I_D R_s = 0 \Rightarrow V_{GS} = V_G - I_D R_s$.

S3: calculate $I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$

S4: calculate V_{DS} and V_{GS}.

Applying KVL at the o/p of ckt we get

$V_{DD} - I_D R_D - V_{DS} - I_D R_s = 0$

$\Rightarrow V_{DS} = V_{DD} - I_D R_D - I_D R_s = V_{DD} - I_D(R_D + R_s)$

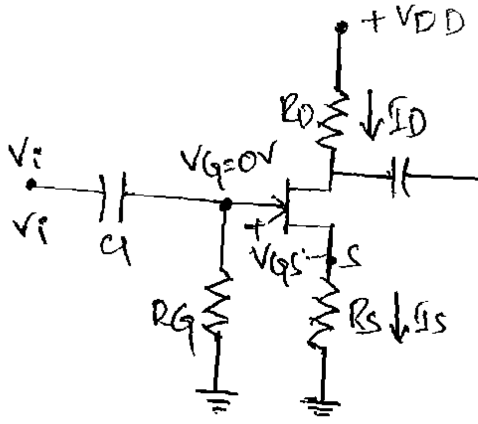
The Q-point of a JFET amplifier using voltage divider bias is

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

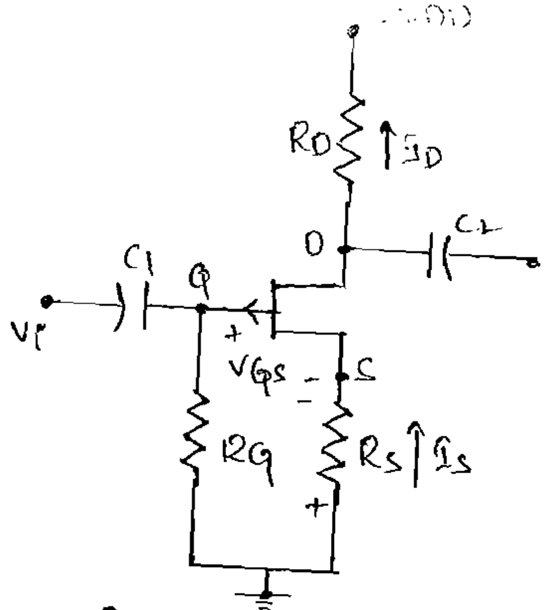
$$V_{DSQ} = V_{DD} - I_D(R_D + R_s)$$

$$V_{GSQ} = V_G - I_D R_s.$$

Self Bias Circuit



n-channel



P-channel

JFET must be operated such that the gate source junction is always reverse biased. This requires a -ve V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. The gate resistor, R_G, doesnot effect the bias because it has essentially no voltage drop across it. so the gate remains at 0V. R_G is necessary only to isolate an a.c. signal from ground in amplifier applications. The voltage drop across R_S make gate source junction reverse biased.

D.C. analysis:

S1: obtain Expression for V_{GS}:

as I_S produces a voltage drop across R_S, and $I_S = I_D$ and $V_G = 0$

then $V_S = I_S R_S = I_D R_S \Rightarrow V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$.

S2: Calculate I_{DQ}

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 = I_{DSS}\left[1 + \frac{I_D R_S}{V_P}\right]^2$$

S3: Calculate V_{DS}.

Applying KVL at o/p we get

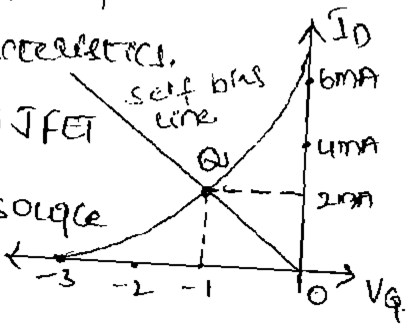
$$V_S + V_{DS} + I_D R_D = V_{DD}.$$

$$\Rightarrow V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D (R_S + R_D)$$

Graphical solution to self bias

for self-bias we know that $V_S = I_D R_S$; $V_{GS} = -V_S = -I_D R_S$

These equations can be used with a transfer characteristics the next fig shows a typical transfer characteristics. (Trans conductance curve) for a self biased JFET the max. drain current is 6mA, and gate to source cutoff voltage is $-3V$.



Now using equation $V_{GS} = -I_D R_S$ and assuming R_S of any suitable value we can draw the self bias line, let assume, $R_S = 500\Omega$

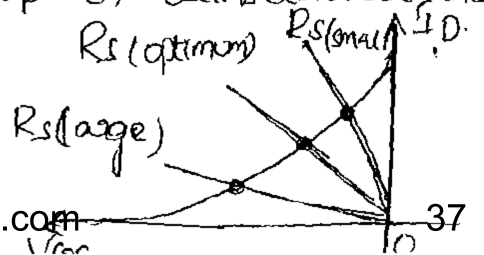
with this R_S we can plot two convenient points corresponding to $I_D = 0$ and $I_D = I_{DSS}$, at first point, $I_D = 0$.

$\therefore V_{GS} = -0(500\Omega) = 0V$ and at second point, $I_D = 6mA$

$\therefore V_{GS} = -(6mA)(500\Omega) = -3V$.

This gives co-ordinates of two points as (0,0) and (6mA, -3V) res. By plotting these two points, we can draw the straight line through the points as shown in above fig. this line will intersect the trans conductance curve and it is known as self bias line. the intersection point gives operating point of the self bias JFET for this circuit. at operating point drain current is slightly greater than 2mA and gate voltage is slightly less than $-1V$.

The Q-point for self bias JFET depends on value of R_S. when R_S is large, the Q-point is far down on transconductance curve, when drain current is small. when R_S is small, the Q-point is far up on trans conductance curve, when drain current is large.

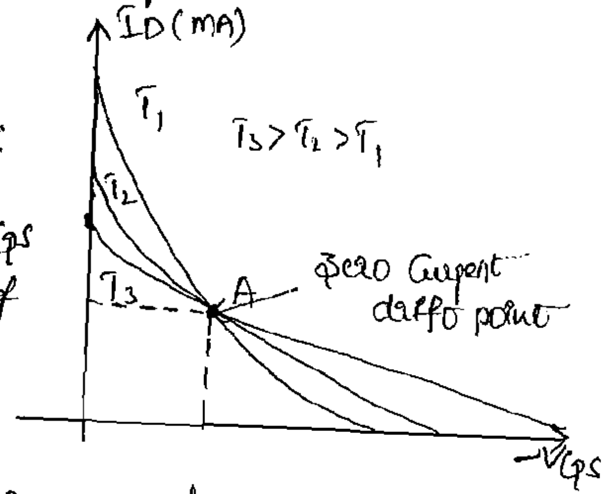


Biasing for zero current drift

In JFET, the drain current varies with changes in temperature due to two factors. One factor increases drain current and other factor decreases drain current with increase in temperature. Therefore it is possible to design biasing circuit which compensates ~~these~~ two factors so that there is no change of drain current with temperature. Such a biasing is called biasing for zero current drift.

1) First factor is the decrease of majority-carrier mobility with increase in temperature. As temperature increases, the lattice ions vibrate more vigorously, and hence carriers cannot move freely in crystalline structure. The reduction in I_D is 0.7% for 1°C increase in temperature.

2) The second factor is the decrease of width of depletion region (i.e. of increase in channel width) with increase in temperature. This allows I_D to increase and increase in I_D is equivalent to a change of 2.2mV/°C in $|V_{GS}|$



Derivation of Condition for zero drift:

Since a change in gate voltage ΔV_{GS} causes a change in drain current of $\Delta I_D = g_m \Delta V_{GS}$, the condition for zero drift is

$$0.007|I_D| = g_m\, 0.0022 \quad (\text{for } 1^\circ C \text{ rise of temperature})$$

$$\Rightarrow \therefore \frac{|I_D|}{g_m} = 0.314V \text{ ; } \quad \text{as we know}$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2 \quad \text{and} \quad g_m = -\frac{2I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]$$

[illegible] $\frac{V_{GS}}{V_P}$ / $\frac{g_{mo}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$ [illegible]

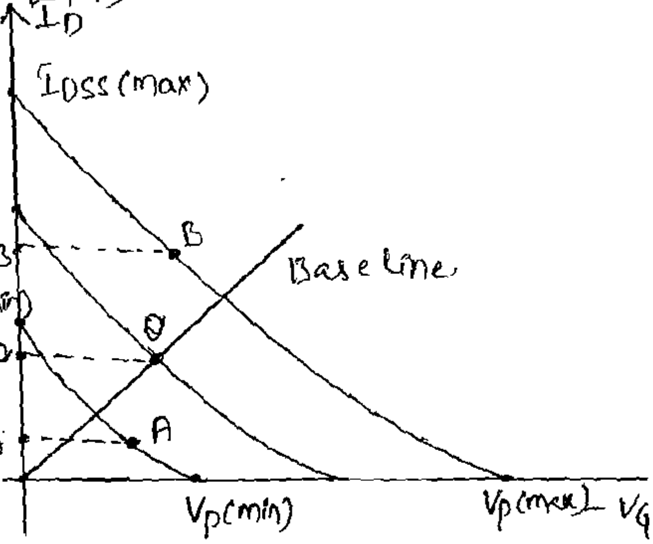
$\Rightarrow |V_P| - |V_{GS}| = -0.628\,V \approx -0.63V.$

from above if we know value of V_P, we can obtain the value of V_{GS} for zero drift current

when V_{GS} is adjusted for zero drift current, I_D and g_m are.

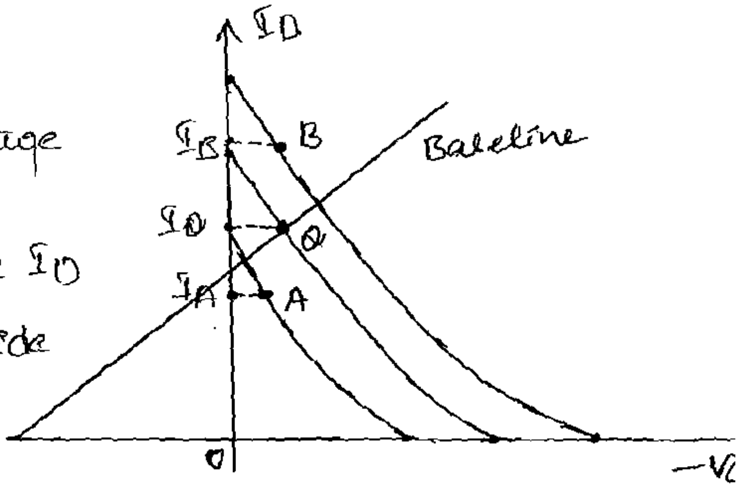
$$I_D = I_{DSS}\left[1-\frac{V_P+0.63}{V_P}\right]^2 = I_{DSS}\left[\frac{0.63}{V_P}\right]^2$$

$$g_m = g_{mo}\left[1-\frac{V_P+0.63}{V_P}\right] = g_{mo}\left[\frac{0.63}{|V_P|}\right]$$



Biasing against device variation.

FET manufacturers usually specify information on the maximum and minimum values of I_{DSS} and V_P at room temperature. they also specify data to correct these quantities for temperature variations. the top and bottom curves are for extreme values of temperature and device variations.



let assume I_D is not allowed to drift outside $I_D = I_A$ and $I_D = I_B$. then the base line $V_{GS} = -I_D R_S$ must intersect the transfer characteristics b/w points A and B. I_Q always have values b/w I_A and I_B such that

$I_A < I_Q < I_B$.

[illegible]

A line drawn to pass between points A and B does not pass through the origin. This practical bias line is represented mathematically as $V_{GS} = V_{GG} - I_D R_S$.

Such a bias relationship may be obtained by adding a fixed bias to the gate in addition to the self bias, this requires two power supplies. The self bias circuit with additional voltage divider requires only one power supply.

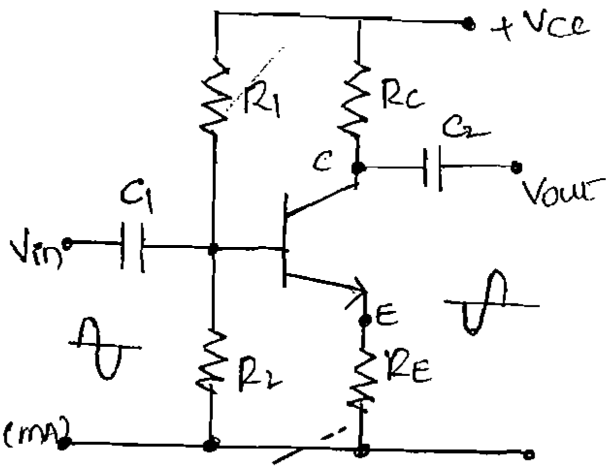
For voltage divider bias $V_{GG} = \frac{R_2}{R_1+R_2} \times V_{DD}$; $R_g = R_1 \| R_2 = \frac{R_1 R_2}{R_1+R_2}$

we assumed that gate current is negligible. It is also possible for V_{GG} to fall in the -ve biased region so that the line in (b) intersects the horizontal axis to the right of origin. Under these circumstances two separate supply voltages must be used.

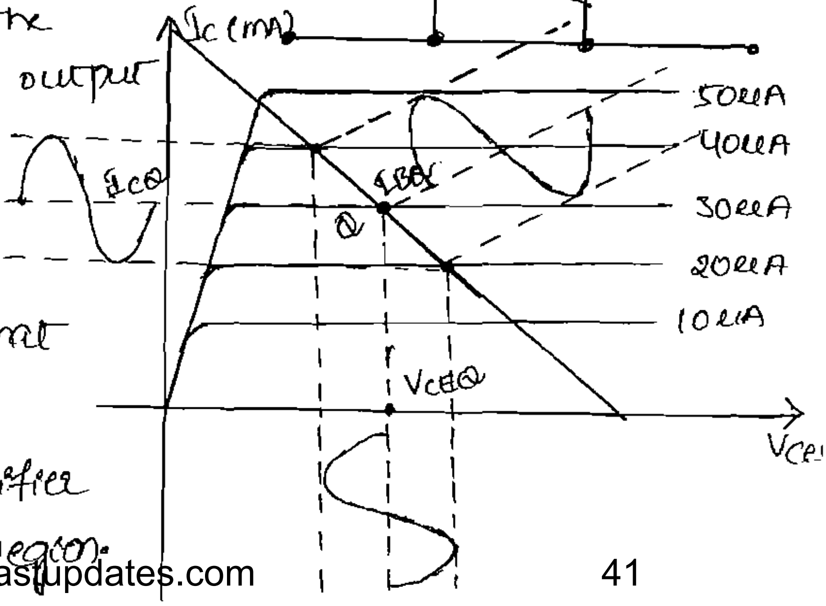
we know that V-I characteristics of an active device such as BJT are nonlinear, with complicated analysis procedure. To simplify analysis of BJT its operation is restricted to linear V-I characteristics around Q-point. i.e. in active region. this is possible only with small i/p signals. the term small signal amplifier refers to the use of signal that takes up a relatively a small percentage of an amplifier's operational range. with small signals the transistor can be replaced with small signal linear model. This model is also called small signal equivalent circuit.

we know that reactance of a capacitor is $X_C = \frac{1}{2\pi fC}$. for low frequencies the values of junction capacitors are very high, as they appear in parallel with junctions, their effect is ignored at low frequencies and analysis is further simplified.

CE, CB and CC Amplifiers:



The amplifier is used to get a larger signal output from a small signal input. we will assume a sinusoidal signal at the i/p of amplifier. At the output signal must remain sinusoidal in wave form with frequency same as that of input. To make the transistor work as an amplifier it is to be biased in active region.



Consider Common emitter amplifier ckt using self bias (or) voltage divider bias

In the absence of i/p signal, only d.c. voltage are present in the circuit. This is known as zero-signal (or) no-signal condition (or) quiescent condition for the amplifier. The d.c. collector-emitter voltage, V_{CE}, the d.c. collector current I_C, and d.c. base current I_B is the quiescent operating point for the amplifier. On this d.c. quiescent operating point, we superimpose a.c. signal by application of a.c. sinusoidal voltage at the input due to this base current varies sinusoidally.

Since the transistor is biased to operate in the active region, the output is linearly proportional to the i/p. I_C is β times larger than i/p base current I_B in CE configuration. Hence collector current will also varies sinusoidally about its quiscent value, I_{CQ}. The output voltage will also vary sinusoidally.

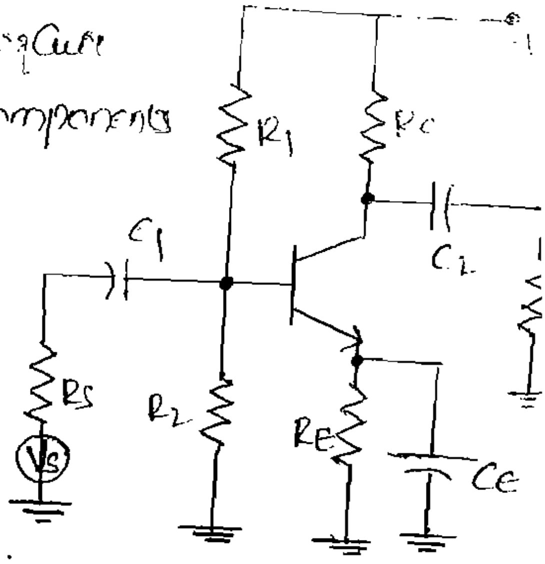
The collector current varies above and below its Q point value in-phase with the base current, and the collector to emitter voltage varies above and below its Q-point value ~~out~~-phase (180°) with base voltage.

When one cycle of i/p is completed, one cycle of output will also be completed. This means the frequency of output sinusoidal is same as the frequency of i/p sinusoid. Thus in amplification process, frequency of o/p signal does not change. Only the magnitude of o/p is larger than that of i/p signal.

The CE Amplifier consists of different circuit components, the functions of these components are

1). Biasing Circuit:

the Resistances R_1, R_2 and R_E form the voltage divider biasing circuit for the CE Amplifier. it sets proper operating point for the CE Amplifier.



2). Input Capacitor C_1:

This Capacitor Couples the signal to the base of the transistor. It blocks any d.c. component present in the signal and passes only a.c. signal for amplification. because of this biasing conditions are maintained constant.

3) Emitter Bypass capacitor C_E:

An Emitter bypass capacitor C_E is connected in parallel with emitter Resistance, R_E to provide a low reactance path to the amplified a.c. signal. If C_E is not inserted, the amplified a.c. signal passing through R_E will cause a voltage drop across R_E. this will reduce o/p voltage, reducing gain of amplifier

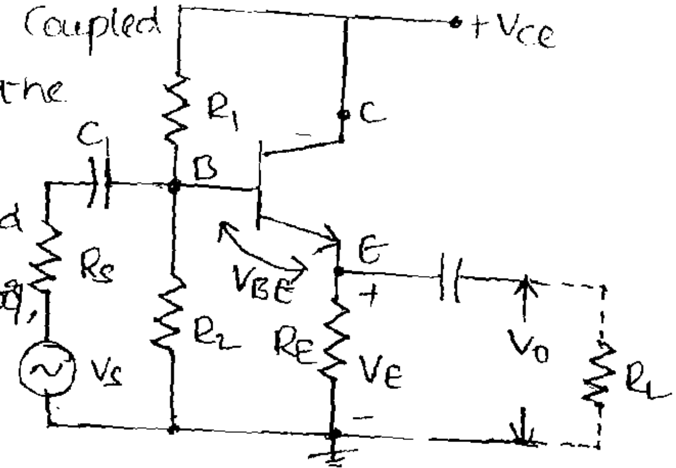
4). Output Coupling capacitor C_2:

C_2 Couples the output of the amplifier to the load (or) to the next stage of amplifier. it blocks d.c. and passes only a.c. part of amplified signal.

the coupling capacitors acts as open circuit for d.c. and short circuit for a.c. components.

Common Collector Amplifier Circuit:

The d.c. biasing is provided by R_1, R_2 and R_E. The load resistance is capacitor coupled to the emitter terminal of the transistor.

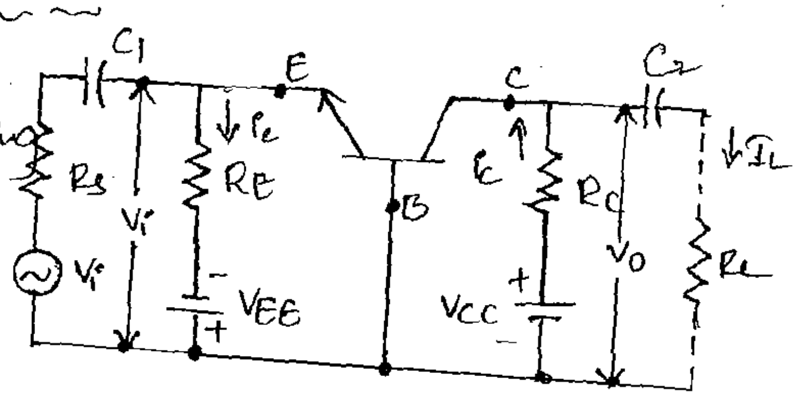


When a signal is applied via to the base of the transistor, V_B is increased and decreased as the signal goes +ve & −ve.

We can note that $V_E = V_B - V_{BE}$, considering V_{BE} fairly constant, we can say that variations in the V_B appears at emitter, and emitter voltage V_E will vary same as base voltage V_B. It can be noted that o/p voltage from a common collector circuit is same as i/p voltage. Hence common collector circuit is also known as emitter follower.

Common Base Amplifier Circuit:

Signal source is connected to the emitter via coupling capacitor C_1.



Load resistor is connected to collector via coupling capacitor C_2.

The positive going pulse of i/p source increases emitter voltage. As base voltage is const., the forward bias of J_E junction reduced. This reduces I_B, hence I_C hence drop across R_C. Since $V_0 = V_{CC} - I_C R_C$, the reduction in I_C results increase in V_0. So positive going i/p produces positive going o/p hence there is no